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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,543	09/30/2003	Jerrell Hein	026-0035	5968

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EXAMINER	
CHANG, JOSEPH	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/675,543	HEIN ET AL.	
	Examiner	Art Unit	
	Joseph Chang	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/18/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 6, 7, 10, 16, 17, 19, 21, 22, 26-28, and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Walker et al., US Patent 5,579,348.

Regarding claim 1, Walker et al. discloses a method comprising: receiving a calibration clock over a terminal (50); generating at least one control value in a control loop to lock a clock (column 5, lines 43-46) generated by a controllable oscillator (20) to a multiple of the calibration clock (34, it is noted that phase is locked with harmonics of clock frequency); and storing a value corresponding to the at least one control value in a non-volatile memory (column 5, lines 43-46). It is inherent that the memory 62 is a non-volatile because of its functionality of data usage and handling.

Regarding claim 2, Figure 2 shows a PLL (column 6, lines 6-7).

Regarding claim 6, PLL is locked to the calibration clock during receipt of the calibration clock (column 5, line 49 - column 6, line 7).

Regarding claim 7, PLL inherently locks phase of integer and fractional multiple of the calibration clock.

Regarding claims 10, 21, 22, 26 and 42, Walker et al. discloses a fixed frequency reference source to synthesize the output clock (column 3, lines 60-63).

Regarding claim 16, 27, Figure 1 shows switches (46 and 50) that selectively coupling the controllable oscillator (20) to a feedback path to form the PLL.

Regarding claim 17, the controllable oscillator (20) is supplied a digital control value (Initial Value) via DAC 26.

Regarding claim 19, Figure 1 shows a switch (46) for disabling a VCXO (20, column 4, line 3) mode of operation prior to providing the calibration clock.

Regarding claim 28, Figure 1 shows memory inherently capable of storing a history of correction factors.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 3-5, 20, and 44-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al. in view of Sutardja US Pub 20040071029.

Regarding 3-5, 44-47, as discussed above, Walker et al. discloses a method and an apparatus of clock circuit including storing a control value in a non-volatile memory. However, walker et al does not explicitly disclose that a second control value be a temperature storing in the non-volatile memory, NVM. As would have been well known in the art, such an additional control value (temperature) be stored in the memory and use it for compensation, for example, shown in Sutardja. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to utilize such temperature value storing in a NVM because such a modification would have provided the benefit of temperature compensation for more stable clock frequency. Regarding claim 20, disabling a temperature compensation mode of operation prior to providing the calibration clock would have been obvious based on the consideration of controlling variations.

Claims 11-15, 18, 20, 23-25, 29-41, 43 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al. in view of Torode, US Patent 5451912.

Regarding claims 11-13, 23, 24, 29 as discussed above, Walker et al. discloses a method and an apparatus of clock circuit including fixed frequency reference source, PLL and calibration clock terminal. However, walker et al does not explicitly disclose that the fixed frequency reference source being a crystal, or the fixed frequency reference source and the PLL being in a sealed package, or the terminal being used for

receiving command sequence. As would have been well known in the art, crystals are stable frequency source and the package is for protection and terminal is to receive signals. Torode teaches that the crystal is enclosed within the package and provides a source frequency, and the PLL circuit, also enclosed in the package, receives the source frequency to produce desired output frequency. And also, the device of Torode has dedicated programming connections to receive a digital command. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to utilize such features as taught by Torode because such a modification would have provided the benefits of protection, stable frequency source and accessibility from external command to control the clock circuit of Walker et al.

Regarding claims 14, 25, such method of determining a divider value would have been obvious because it is necessary step upon channel selections.

Regarding claims 15, 32, 41, Figure 1 shows the terminal 50 is a bi-direction (42).

Regarding claim 18, setting a voltage control input to midrange would have been obvious based on the optimization range. Therefore, it would have been obvious to one of ordinary skill in the art.

Regarding claim 20, disabling a temperature compensation mode of operation prior to providing the calibration clock would have been obvious based on the consideration of controlling variations.

Regarding claim 30, 35-37, 43, 48, the apparatuses in an IC would have been obvious based on the miniaturization and mass production considerations.

Regarding claim 31, the terminal being a pin on a package holding a semiconductor device would have been obvious because it is necessary to hold the circuit in the package.

Regarding claims 33-34, 40, Walker et al. discloses a control circuit as recited in the claim (column 2, lines 49-67, 23-49).

Regarding claim 39, the package being a ceramic would have been obvious because of well-known material for the package in semiconductor manufacture art and for its firmness to protect the circuit inside.

Response to Arguments

Applicant's arguments with respect to claims 1-48 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Chang whose telephone number is 571 272-1759. The examiner can normally be reached on Mon-Fri 0700-1730.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph Chang
Patent Examiner
Art Unit 2817